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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/815,746	04/02/2004	Kuo-Yu Chou	BHT-3212-56	1557

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EXAMINER	
MAI, LAM T	

ART UNIT	PAPER NUMBER
2819	

MAIL DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/815,746	CHOU, KUO-YU	
	Examiner	Art Unit	
	LAM T. MAI	2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 April 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 and 12* is/are rejected.

7)☒ Claim(s) *2-11 and 13-22* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Specification

The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1 and 12 are rejected under 35 U.S.C. 102(e) as being anticipated by Rossi (USP 6,753,801).

Regarding claim 1, Rossi discloses in figures 4a-4d an ADC architecture that teaches:

a variable gain amplifier circuit (554) comprising a first input end (552), a second input end (556), and at least one output end (560 or 562), the first input end being used for receiving the first voltage level signal, the second input end being used for receiving

the first reference signal, the output end being used for outputting at least an amplified signal,

a first sample switch (542) in the front end of the first input end,

a second sample switch (544) in the front end of the second input end, and

a hold switch (550)connected between the first input end and the second input end,

wherein while the first sample switch is at a first conductive state, the first input end receives the first voltage level signal, while the second sample switch is at the first conductive state, the second input end receives the first reference signal, and while the hold switch is at a second conductive state, the output end outputs the amplified signal; and

an analog to digital converter device (100 in figure 9) for receiving the amplified signal and converting the amplified signal into the digital signal. (see figure 6-8 and their descriptions).

Regarding claim 12, Rossi discloses in figures 4a-4d an ADC architecture technique that teaches steps:

(a) receiving the first voltage level signal by a first input end of a variable gain amplifier circuit (554) when a first sample switch (542) in the front end of the first input end is set at a first conductive state;

(b) receiving the first reference signal by a second input end of the variable gain amplifier circuit (554) when a second sample switch (544) in the front end of the second input end is set at the first conductive state;

(c) outputting at least one amplified signal (560 or 562) via an output end of the variable gain amplifier circuit (554_ when a hold switch (550) connected between the first input end and the second input end is at a second conductive state; and

(d) converting (by device 100 in figure 9) the amplified signal (560 or 562) into the digital signal . (see figure 6-8 and their descriptions as well).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 1 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakamura et al. (USP 7,123,301) and further in view of Rossi (USP 6,753,801).

Regarding claim 1, Nakamura discloses in figures 4 and 6 that teaches an ADC (404) coupled to the VGA (404) for converting the amplified signal into a digital signal. Nakamura silent about the detail of how the input signal be amplified. While Rossi discloses in figures 4a-4d an architecture that teaches how the input signal be amplified as follow:

a variable gain amplifier circuit (554) comprising a first input end (552), a second input end (556), and at least one output end (560 or 562), the first input end being used for receiving the first voltage level signal, the second input end being used for receiving the first reference signal, the output end being used for outputting at least an amplified signal,

a first sample switch (542) in the front end of the first input end,

a second sample switch (544) in the front end of the second input end, and

a hold switch (550)connected between the first input end and the second input end,

while the first sample switch is at a first conductive state, the first input end receives the first voltage level signal, while the second sample switch is at the first conductive state, the second input end receives the first reference signal, and while the hold switch is at a second conductive state, the output end outputs the amplified signal.

It would have been obvious to one of ordinary skill in the art to implement technique how the input be amplified taught by Rossi into Nakarmura's invention to satisfy or improve design's need or design's requirement.

Regarding claim 12, Nakamura discloses in figures 4 and 6 that teaches an technique converting (via ADC 404) amplified signal (via VGA 402) into a digital signal. Nakamura silent about the detail of how the input signal be amplified. While Rossi discloses in figures 4a-4d an architecture that teaches how the input signal be amplified as follow:

(a) receiving the first voltage level signal by a first input end of a variable gain amplifier circuit (554) when a first sample switch (542) in the front end of the first input end is set at a first conductive state;

(b) receiving the first reference signal by a second input end of the variable gain amplifier circuit (554) when a second sample switch (544) in the front end of the second input end is set at the first conductive state;

(c) outputting at least one amplified signal (560 or 562) via an output end of the variable gain amplifier circuit (554_ when a hold switch (550) connected between the first input end and the second input end is at a second conductive state;

It would have been obvious to one of ordinary skill in the art to implement technique how the input be amplified taught by Rossi into Nakarmura's invention to satisfy or improve design's need or design's requirement.

Allowable Subject Matter

Claims 2-11 and 13-22 are objected to as being dependent upon a rejected base claim, but they would be considered for allowable if they are rewritten in independent form including all of the limitations of the base claim and any intervening claims. Features of objected claims are not taught or suggested in the prior art of record.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to LAM T. MAI whose telephone number is (571)272-1807. The examiner can normally be reached on 5:30 am - 4:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Barnie Rexford can be reached on (571) 272-7492. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Lam T. Mai
Primary Examiner
Art Unit 2819